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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/651,385	08/29/2000	Sanjay Dabral	042390.P5258D	9681

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EXAMINER	
DIAZ, JOSE R	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 01/25/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/651,385	DABRAL ET AL.	
	Examiner	Art Unit	
	José R. Díaz	2815	

-- The MAILING DATE of this communication appears on the cover sh et with the correspondenc address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 November 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *20-23 and 26-36* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *20-23 and 26-36* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on November 12, 2004 has been entered.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 20-23 and 26 are rejected under 35 U.S.C. 102(b) as being anticipated by Marum et al. (US Pat. No. 5,500,546).

Regarding claim 20, Marum et al. teaches a method of forming an integrated circuit comprising:

forming a performance circuit (20) occupying a first well of an integrated circuit substrate (see fig. 2); [1]

[1] With regards to the claimed first well, Marum et al. teaches that the performance circuit (20) is a CMOS device (col. 3, lines 27-28). It is very well known in the art that a CMOS device inherently include wells or tubs, since such wells or tubs are required to accommodate both nMOS and pMOS transistors on the same substrate.

forming a protection circuit (14) (see fig. 2) occupying a second well (34) of the integrated circuit substrate separate from the first well [2], wherein forming the protection circuit includes:

forming a plurality of unit cells (consider the P-type squares shown in figure 4), the plurality of unit cells separated from each other to form a plurality of islands in the second well (34), surrounded by the second well (consider the P-type squares surrounded by the Z-well (34) shown in figure 4), each of the plurality of unit cells comprised of:

a block of a first doped region (72) of a first dopant in the second well (34) the integrated circuit substrate occupying an area of the substrate sufficient to support a contact to the first doped region, the first doped region forming an anode of a diode (70) (see figs. 4 and 4a.),

a junction region of the integrated circuit substrate surrounding the first doped region (72) and separating the first doped region (72) from the second well (34) (consider the boundary lines that enclosed the P-type region 72 in figures 4 and 4a), and

a contact to the first doped region (72) [please note that the doped regions 72 constitute the anode contacts of the diode 70 (see fig. 4), which are connected or coupled to a ground potential. See col. 9, lines 5-7 and col. 9, lines 44-58];

[2] With regards to forming the second well separate from the first well, it is noted that the second well (34) shown in figure 4 does not include the CMOS device (20) shown in figure 2. Thus, it is inherent that the second well (34) is formed separate from the wells of the CMOS device (20).

the second well (34) is doped with a first concentration of a second dopant (N+) (see fig. 4a and col. 3, lines 10-18);

forming a third doped region (71) in the second well (34) adjacent the junction region (see fig. 4a), the third doped region surrounding the plurality of cells and doped with a second concentration of the second dopant (N) (see col. 3, lines 57-59), the third doped region forming a cathode of the diode (See col. 5, lines 51-54 and col. 9, lines 5-6, wherein Marum et al. states that region 36, which is analogous to region 71, "forms the cathode contact."); and

coupling the protection circuit (14) to the performance circuit (20) (see col. 1, lines 60-63).

Regarding claim 21, Marum et al. further teaches that the performance circuit (20) includes forming a CMOS configuration (see col. 3, lines 27-28).

Regarding claims 22-23, Marum et al. further teaches wherein includes forming the protection circuit (14) includes a diode (70) (see col. 3, lines 54-56) and coupling the protection circuit (14) to the performance circuit (20) includes coupling the protection circuit to a p-channel device (p-MOS) of the CMOS configuration (see col. 3, lines 4-6, 29-31 and 55-57).

Regarding claim 26, Marum et al. further teaches forming a plurality of unit diodes (consider the squares enclosed by region 71 in figure 4).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

6. Claims 27-29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Marum et al. (US Pat. No. 5,500,546) in view of Ker et al. (US Pat. 5,714,784).

Regarding claim 27, Marum et al. teaches a method of forming an integrated circuit comprising:

forming a first protection circuit (14) on the integrated circuit substrate (see fig. 2);

forming a performance circuit (20) occupying a first well of an integrated circuit substrate (see fig. 2). [With regards to the first well, Marum et al. teaches that the performance circuit (20) is a CMOS device (col. 3, lines 27-28). It is very well known in

the art that a CMOS device inherently include wells or tubs, since such wells or tubs are required to accommodate both nMOS and pMOS transistors on the same substrate],

forming a protection circuit (40) (see fig. 3) occupying a second well (34) of the integrated circuit substrate (see fig. 3c) separate from the first well [please note that the device (60) formed in the well (34) does not include the CMOS device (20) (see figures 3c and 3d), thus it is inherent that the second well (34) is separated from the well of the CMOS device (20)], the protection circuit including a plurality of unit cells (62, 64) forming a plurality of islands in the second well (34) surrounded by a doped region (32) (see figure 3c); and

coupling the protection circuit (40) to the performance circuit (20) (see figure 3).

However, Marum et al. fails to teach the step of forming a performance circuit by forming a unit transistor device having a drain region comprised of a doped region of the integrated circuit substrate occupying an area sufficient to support a contact to the doped region; forming a gate region of the integrated circuit substrate surrounding the doped region; and forming a contact to the doped region.

Ker et al. teaches that it is well known in the art to form the performance circuit by forming a unit transistor (figure 4 and abstract) device having a drain region (41) comprised of a doped region of the integrated circuit substrate occupying an area sufficient to support a contact (46) to the doped region (see fig. 4); forming a gate region (42) of the integrated circuit substrate surrounding the doped region (41) (see fig. 4); and forming a contact to the doped region (46) (see fig. 4).

Marum et al. and Ker et al. are analogous art because they are from the same field of endeavor as applicant's invention. At the time of the invention it would have

been obvious to a person of ordinary skill in the art to include the steps of: forming a unit transistor device having a drain region comprised of a doped region of the integrated circuit substrate occupying an area sufficient to support a contact to the doped region; forming a gate region of the integrated circuit substrate surrounding the doped region; and forming a contact to the doped region. The motivation for doing so, as is taught by Ker et al., is reducing total layout area and to cut cost (col. 4, lines 5-9). Therefore, it would have been obvious to combine Ker et al. with Marum et al. to obtain the invention of claims 27-29.

Regarding claim 28, Ker et al. further teaches that the doped region (41) being a first doped region of a first dopant (see fig. 4) in a well of the substrate (see col. 4, lines 15-17), the well being doped with a concentration of a second dopant (see col. 4, lines 15-17) and wherein forming a performance circuit further comprises: forming a source region (43) of the transistor doped with the first dopant in the well separated from the drain region by the gate to form a unit transistor (see fig. 4).

Regarding claim 29, Ker et al. further teaches that forming a performance circuit includes: forming a plurality of unit transistors (consider the squares surrounded by region 43 in fig. 4).

7. Claims 30-36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Marum et al. (US Pat. No. 5,500,546) in view of Beasom (US Pat. No. 5,448,100).

Regarding claims 30, 35 and 36, Marum et al., as stated in the rejection of claim 20, teaches the claimed method except for the limitation that the third doped region has a second concentration of the second dopant that is greater than the first concentration

of the second well. However, Beasom teaches that it is well known in the art to form the third doped region (18) having a concentration of the second dopant (N+) greater than the first concentration (N) of the second well (12) (see fig.1 and col. 2, lines 48-52).

Marum et al. and Beasom are analogous art because they are from the same field of endeavor as applicant's invention. At the time of the invention it would have been obvious to a person of ordinary skill in the art to form the third doped region having a second concentration of the second dopant greater than the first concentration of the second well. The motivation for doing so, as is taught by Beasom, is to reduce series resistance of the diode (col. 2, lines 63-66). Therefore, it would have been obvious to combine Beasom with Marum et al. to obtain the invention of claims 30-36.

Regarding claim 31, Marum et al. further teaches that the performance circuit (20) includes forming a CMOS configuration (see col. 3, lines 27-28).

Regarding claims 32-33, Marum et al. further teaches wherein includes forming the protection circuit (14) includes a diode (70) (see col. 3, lines 54-56) and coupling the protection circuit (14) to the performance circuit (20) includes coupling the protection circuit to a p-channel device (p-MOS) of the CMOS configuration (see col. 3, lines 4-6, 29-31 and 55-57).

Regarding claim 34, Marum et al. further teaches forming a plurality of unit diodes (consider the squares enclosed by region 71 in figure 4).

Response to Arguments

8. Applicant's arguments filed November 12, 2004 have been fully considered but they are not persuasive.

Applicant argues that the doped region 71 in Marum et al. is not a "cathode". However, this argument is not persuasive. It is noted that Applicant uses the label "cathode" to identify the contact doped region 160 (see fig. 8), which is also taught by Marum et al. as the doped region 71 (see fig. 4). Thus, the term "cathode" is merely a label given by Applicant to a doped region formed by the instance method and does not distinguish over the doped region (71) taught by Marum et al. As such, Marum et al. does teach and therefore anticipates the claimed doped region.

In addition, Applicant argues that the combination of Marum et al. and Kerr does not teach a second protection circuit between a first protection circuit and a performance circuit. However, this argument is not persuasive in view of the rejection provided above.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The following references teach a zener diode as the protection circuit: Chen et al. (US Pat. No. 5,869,882), figs. 1and 2; Wang et al. (US Pat. No. 6,365,924 B1), figs. 9A-9B; Worley et al. (US Pat. No. 5,440,162, figs. 5-6; Voldman et al. (US Pat. No. 5,629,544), see fig. 3d; Ono (US Pat. No. 5,796,147), fig. 16; Duvvury (US Pat. No. 5,502,317), figs. 1 and 3; and Zambrano (US Pat. No. 5,426,320).

Correspondence

Any inquiry concerning this communication or earlier communications from the examiner should be directed to José R. Díaz whose telephone number is (571) 272-1727. The examiner can normally be reached on Monday through Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (571) 272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

1/24/05

José R. Díaz
Examiner
Art Unit 2815